REMARKS

The Remarks are in response to the communication dated on the Office Communication mailed on mailed on January 24, 2007, having a one-month, non-extendable response time. The Communication rejected claims 42 and 43, but required compliance with 37 CFR §41.202(a).

Consequently, in response to the various portions of 37 CFR §41.202(a):

(1) Identification of Patent

Section (1) requires sufficient information to identify the patents with which the interference is sought.

Claims 42 and 43 are respectively exact or close copies of 1 and 2 of U.S. patent number 6,538,923 of Parker, granted March 25, 2003.

(2) Identification of Claims Believed to Interfere, Proposed Count, and Claim Correspondence

Section (2) requires that all claims believed to interfere are identified, that one or more counts is proposed, and that it is shown how the claims correspond to the one or more counts.

Claims 42 and 43 are respectively exact or close copies of 1 and 2 of U.S. patent number 6,538,923 and, consequently, so correspond.

Claim 42 of the present application, which is an exact copy of claim 1 of U.S. patent number 6,538,923, is suggested as Count 1:

Count 1

A non-volatile semiconductor memory device, comprising:

a memory array including a plurality of multi-level-cell memory cells, each memory cell comprising a storage element having a capacity to store N bits of logical data,

where $N \geq 2$, and each memory cell configured for 2^N distinct data storage levels, each of the 2^N data storage levels representative of a discrete N-bit combination of logical data; and

a staircase program-verify circuit for providing a staircase program-verify pulse electrically coupled to the memory array and capable of concurrently program-verifying the plurality of multi-level-cell memory cells and inhibiting programming of a memory cell programmed to substantially within a selected data storage level.

Claim 43 of the present application, which is an exact copy of claim 2 of U.S. patent number 6,538,923, is suggested as Count 2:

Count 2

The device of Count 1, wherein the storage element comprises a semiconductor transistor having a programmable threshold voltage, V_t, within a continuous range from a lowest V_t value to a highest V_t value, the continuous range having 2^N distinct data storage levels including an erased level and 2^N-1 program levels, the 2^N-1 program levels including a lowest program level, at least one intermediate program level, and a highest program level.

(3) Claim Chart for the Counts

As the proposed Count 1 is both Claim 42 of the present application and an exact copy of claim 1 of U.S. patent number 6,538,923, they correspond exactly:

Claim 42 of Present Application	Count 1
42. A non-volatile semiconductor memory device, comprising:	A non-volatile semiconductor memory device, comprising:
a memory array including a plurality of multi-level-cell memory cells, each memory cell comprising a storage element having a capacity to store N bits of logical data,	a memory array including a plurality of multi-level-cell memory cells, each memory cell comprising a storage element having a capacity to store N bits of logical data,
where $N \geq 2$, and each memory cell configured for 2^N distinct data storage levels, each of the 2^N data storage levels representative of a discrete N-bit combination of logical data; and	where $N \geq 2$, and each memory cell configured for 2^N distinct data storage levels, each of the 2^N data storage levels representative of a discrete N-bit combination of logical data; and
a staircase program-verify circuit for providing a staircase program-verify pulse electrically coupled to the memory array and capable of concurrently program-verifying the plurality of multi-level-cell memory cells and inhibiting programming of a memory cell programmed to substantially within a selected data storage level.	a staircase program-verify circuit for providing a staircase program-verify pulse electrically coupled to the memory array and capable of concurrently program-verifying the plurality of multi-level-cell memory cells and inhibiting programming of a memory cell programmed to substantially within a selected data storage level.

Claim 1 of U.S. patent number 6,538,923	Count 1
42. A non-volatile semiconductor memory device, comprising:	A non-volatile semiconductor memory device, comprising:
a memory array including a plurality of multi-level-cell memory cells, each memory cell comprising a storage element having a capacity to store N bits of logical data,	a memory array including a plurality of multi-level-cell memory cells, each memory cell comprising a storage element having a capacity to store N bits of logical data,
where $N \geq 2$, and each memory cell configured for 2^N distinct data storage levels, each of the 2^N data storage levels representative of a discrete N-bit combination of logical data; and	where $N \geq 2$, and each memory cell configured for 2^N distinct data storage levels, each of the 2^N data storage levels representative of a discrete N-bit combination of logical data; and
a staircase program-verify circuit for providing a staircase program-verify pulse electrically coupled to the memory array and capable of concurrently program-verifying the plurality of multi-level-cell memory cells and inhibiting programming of a memory cell programmed to substantially within a selected data storage level.	a staircase program-verify circuit for providing a staircase program-verify pulse electrically coupled to the memory array and capable of concurrently program-verifying the plurality of multi-level-cell memory cells and inhibiting programming of a memory cell programmed to substantially within a selected data storage level.

As the claims are identical and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

As the proposed Count 2 is both Claim 43 of the present application and an exact copy of claim 2 of U.S. patent number 6,538,923, they correspond exactly:

Claim 43 of Present Application	Count 2
43. The device of claim 42, wherein the storage element comprises a semiconductor transistor having a programmable threshold voltage, V_t, within a continuous range from a lowest V_t value to a highest V_t value, the	The device of Count 1, wherein the storage element comprises a semiconductor transistor having a programmable threshold voltage, V_t, within a continuous range from a lowest V_t value to a highest V_t value, the

continuous range having 2^N distinct data storage levels including an erased level and 2^N-1 program levels, the 2^N-1 program levels including a lowest program level, at least one intermediate program level, and a highest program level.	continuous range having 2^N distinct data storage levels including an erased level and 2^N-1 program levels, the 2^N-1 program levels including a lowest program level, at least one intermediate program level, and a highest program level.

Claim 2 of U.S. patent number 6,538,923	Count 2
2. The device of claim 1, wherein the storage element comprises a semiconductor transistor having a programmable threshold voltage, V_t, within a continuous range from a lowest V_t value to a highest V_t value, the continuous range having 2^N distinct data storage levels including an erased level and 2^N-1 program levels, the 2^N-1 program levels including a lowest program level, at least one intermediate program level, and a highest program level.	The device of Count 1, wherein the storage element comprises a semiconductor transistor having a programmable threshold voltage, V_t, within a continuous range from a lowest V_t value to a highest V_t value, the continuous range having 2^N distinct data storage levels including an erased level and 2^N-1 program levels, the 2^N-1 program levels including a lowest program level, at least one intermediate program level, and a highest program level.

As the claims are again identical and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

(4) How Applicant Will prevail on Priority

The present application is a continuation of U.S. patent application serial no. 10/013,592, filed November 13, 2001; which is a continuation of U.S. patent application serial no. 09/688,061, filed October 13, 2000, now U.S. patent no. 6,317,364; which is a division of application serial no. 08/910,947, filed August 7, 1997, now U.S. patent no. 6,222,762. .Consequently, the present application is entitled to a priority date of August 7, 1997.

U.S. patent number 5,619,451 has a filing date of February 26, 2001, over three years later than the August 7, 1997 filing date to which the present application is entitled.

(5,6) Claim Charts

The following claim charts show the corresponding written description for each claim in the specification of the present application. They also show where the disclosure provides a constructive reduction to practice within the scope of the interfering subject matter.

Support for Claims

42. A non-volatile semiconductor memory device, comprising:	See "Field of the Invention", page 1, lines 13 and 14.
a memory array including a plurality of multi-level-cell memory cells, each memory cell comprising a storage element having a capacity to store N bits of logical data,	See the first paragraph of the Background section (page 1, lines 17-27), which provides the context for the inventions of the following specification.
where $N \geq 2$, and each memory cell configured for 2^N distinct data storage levels, each of the 2^N data storage levels representative of a discrete N-bit combination of logical data; and	Figures 4a and 4b show the case for N=2 and N=3. An explicit description in terms of n=2^K states is given, for example, on page 20 at line 28.
a staircase program-verify circuit for providing a staircase program-verify pulse electrically coupled to the memory array and capable of concurrently program-verifying the plurality of multi-level-cell memory cells and inhibiting programming of a memory cell programmed to substantially within a selected data storage level.	Multi-state writing and verify techniques are discuss, for example, in the "Multi-State Writing" section, beginning on line 5 of page 18. Figure 8 shows the use of a "Staircase Current Generator" circuit used in the described manner.

43. The device of claim 42, wherein the storage element comprises a semiconductor transistor having a programmable threshold voltage, V_t, within a continuous range from a	(For Claim 42, see above.) That the memory cells use a threshold voltage is described, for example, in the first sentence of the Background (page 1, lines 17-18); the

lowest V_t value to a highest V_t value, the continuous range having 2^N distinct data storage levels including an erased level and 2^N-1 program levels, the 2^N-1 program levels including a lowest program level, at least one intermediate program level, and a highest program level.	continuous range of threshold values and its division into the multi-states is shown for specific examples in Figures 4a and 4b; and that these include an erased level is disclosed, for example, on lines 19-20 of page 19.

Conclusion

As presented above, it is respectfully submitted that the present application supports all of the currently pending claims and that the requirements of 37 CFR §41.202(a) have been met. A phone call to the undersigned is invited should there be any questions.

Respectfully submitted,

2/23/07

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